Specification Amendments

Please replace the paragraph [006] with the following rewritten paragraph:

[006] Wirebonding is the most common technique for establishing electrical connection between the bonding pads on the surface of a chip or die and the inner lead terminals, or posts, on the leadframe or substrate. A section of a typical conventional wirebonded chip 26 is shown schematically in Fig. 1 and may include multiple wire bonding balls 10, each of which is directly bonded to the continuous upper surface of a bonding pad 14, typically rectangular in configuration, as shown in Fig. [[1A]]2, and partially covered by a passivation layer 12. A pad opening 13 in the passivation layer 12 exposes the bonding pad 14, through which pad opening 13 the bonding ball 10 extends. The bonding pad 14 is surrounded by a dielectric layer 15 such as an oxide in the chip 26. As further shown in Fig. 1, the bonding pad 14 is provided in electrical contact with an upper conductive layer 16, which is separated from an underlying conductive layer 22 by an insulative layer 18. The conductive layers 16, 22 are disposed in electrical contact with each other through conductive

vias 20 that extend through the insulative layers 18. The various insulative layers 18 and conductive layers 22 are sequentially deposited on a silicon substrate 24 throughout semiconductor fabrication, in conventional fashion. Each bonding ball 10 connects a bonding wire 11 through a lead to the terminals (not shown) on a leadframe.